SEMICON, PACKAGING & ASSEMBLY REPORT
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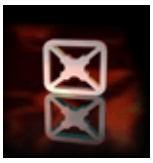
BUSINESS & MARKET NEWS



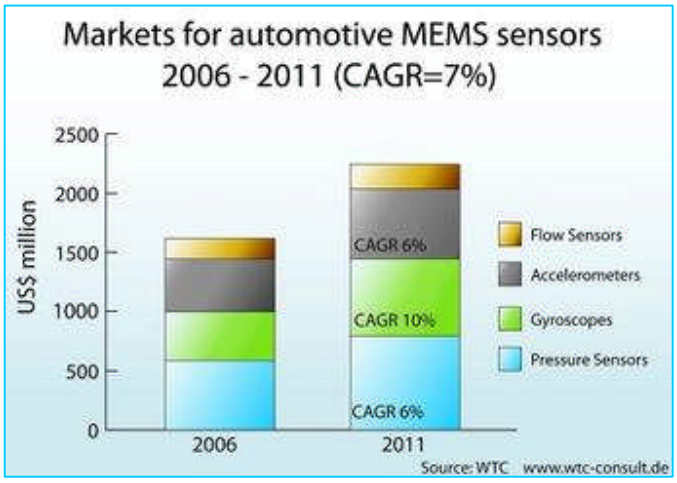
SiTime Goes High Volume - SiTime Corporation announced that their SiT8002 and SiT1 oscillator families are shipping at a production rate of more than 100,000 units per week, making these products the top-selling MEMS-based oscillators worldwide. This milestone represents the start of a new silicon MEMS industry that stands poised to replace a substantial portion of the 10-billion quartz-based oscillators produced annually. Shipping fully qualified MEMS-based oscillators in high volume is a major milestone in the electronics industry. The SiT8002 is the world's smallest programmable oscillator, which allows for fast-turn prototyping, and can be programmed to any frequency between 1 MHz – 125 MHz. The SiT1 fixed frequency oscillators are available in 173 common frequencies and are a low cost solution for high volume customers. Both oscillator products are offered in four package sizes down to 2.5 x 2.0-mm, and are highly reliable, mechanically robust, and low cost compared to competitive quartz solutions. SiTime designs, manufacturers, and markets MEMS-based silicon resonators, oscillators, and complete timing devices. SiTime's primary investors are JAFCO, NEA, Greylock, and Northgate venture capital firms, and Robert Bosch GmbH. Source: Business Wire.

Vietnam Packaging Business - Silicon Valley investors announced adding as much as $200-million into a new chip-packaging plant in Hanoi. The newly formed Vietnam-Chipscale Advanced Packaging Services (V-Caps) will be led by a group of semiconductor executives with valley ties. The nation has 84 million people and is emerging as the new outsource "bargain" shop. Forecasters say that the economy will grow at 9% in 2007. The cost of doing business in Vietnam is about 50% as much as for China. Low cost is not the driving force for going there, but the culture a value system that is based on loyalty, creativity, knowledge, curiosity, tenacity, an advantage over most other countries. The 300,000-square-foot factory will be in the new Hoa Lac High Tech Park and will employ up to 1,500 workers. V-Caps will consider building two more similar facilities, as well. The company will assemble and test chip packages for semiconductor companies for an array of products, from cell phones to personal computers. ***[We'll have to what and see if Vietnam will be the next Asian giant]***. Source: SI.

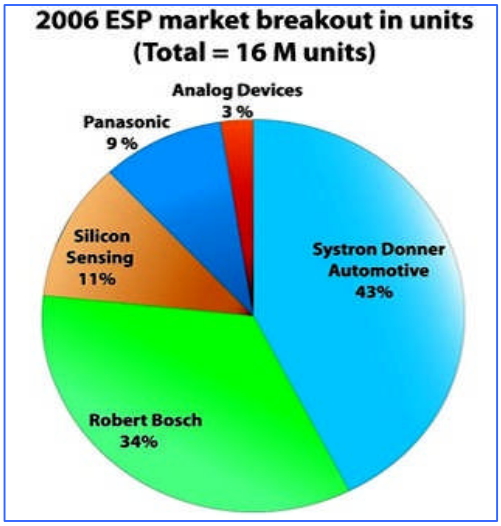
MEMS, NANOELECTRONICS and MOLECULAR ELECTRONICS

MEMS in the Automotive Industry - The automotive sector has long been a growth market for MEMS sensors. However, the industry continues to change and face new opportunities and challenges. Today's high-end vehicles feature up to 100 different sensors; about 30 these are now MEMS. The market is made up of accelerometers, gyroscopes and inclinometers as well as pressure and flow sensors. Emerging

applications include IR sensors for air quality, microscanners for displays and, further out, MEMS oscillators and energy scavengers for TPMS. The automotive sector accounted for $1.6-billion, making this the second biggest MEMS opportunity after IT peripherals and inkjet print heads. By 2011 the market will top $2.2-billion; CAGR ~7%. The main applications in revenues terms are, in order, pressure sensors, gyroscopes, accelerometers and flow sensors and this will remain so for the foreseeable future. The total number of sensors will grow from over 430-million units in 2006 to 780-million in 2011; annual growth of 13%. This outstrips the dollar growth due to price erosion running at 4-5% per year. Leading markets are ESP gyroscopes ($272 million), airbags ($260 million), followed by pressure with MAP and BAP (total $192 million), side airbags and tire pressure monitoring (TPMS). The market for TPMS systems will grow at 50% this year due to a US mandate before leveling off in 2008-2010 to fewer than 10%. Suppliers to this industry include 13 companies from the top 30 MEMS sensor producers (in last month's report). Robert Bosch leads the field and is the 4th biggest MEMS supplier overall with $374-million, up there with giants like Hewlett Packard and Texas Instruments. The airbag market continues to provide impressive unit growth, driven for example by new markets in Asia. Integrators like Autoliv expect airbag penetration to increase from 40 to 60-million vehicles over the next five years (i.e. 80% of cars worldwide). This will equate to insertion from 200-million accelerometers today to 350-million in 5 years, with as many as 8 accelerometers per electronic control unit (ECU). Major players in this space include Bosch, Infineon, Analog Devices, Denso, and Delphi.



Today ESP systems (Electronic Stability/Skid Prevention) make up 2/3 of the revenues for gyroscopes. This amounted to around 16 million units in 2006. Schneider Electric, Robert Bosch, Silicon Sensing Systems and Panasonic dominate this market space. We have now updated our data to take account of the mandatory introduction of such systems in the USA in 2010. Penetration of ESP was below 20-25% in 2006 in the US compared to over 40% in Europe. The US mandate will rapidly accelerate the market for ESP. This is stimulating interest from potential future suppliers; among these are Freescale, Honeywell, Infineon, Sensor Dynamics-

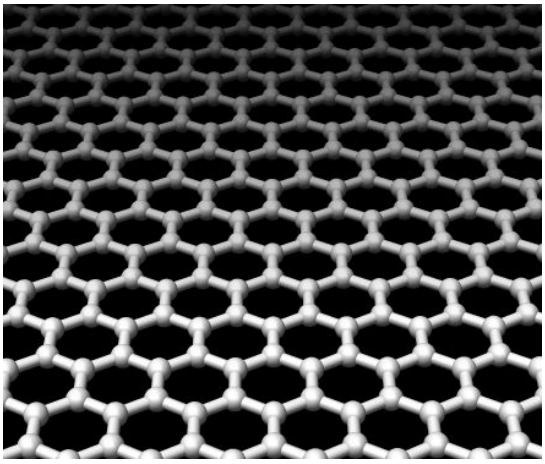


Fraunhofer, and Microcomponents, a Swatch group company with a quartz gyroscope. While not all will succeed we believe there is room for about 7-8 players in total. The number of ESP units will reach 28 million in 2011 or 40% of cars worldwide. ASPs will drop at a rate of 3-4% in the first few years and more sharply after the US law comes into effect prior to 2010. Growth in ESP systems will continue to benefit accelerometer companies like VTI, which supplies low g sensors needed to measure lateral acceleration in a curve, or vertical acceleration in roll detection systems.

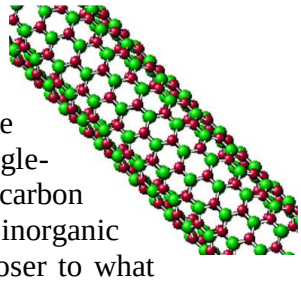
US regulations (TREAD) governing tire pressure monitoring this year will accelerate the pressure sensor market. Undergoing rapid technology iterations, TPMS systems will eventually evolve into smaller, lighter batteryless "intelligent tire" systems that attach to the tire, not the rim. Tires provide a high vibration environment that allows sensor engineers to consider energy harvesting solutions. At the same time, this gives tire makers a chance to add intelligence and move up the value chain. Intelligent tire systems could conceivably add new functionalities such as force, friction/grip, ID and wheel speed to feed ESP systems and other sensor fusion scenarios. We expect intelligent tires with a battery in 2010 and from 2012, intelligent tires powered by MEMS vibration energy scavengers. Such systems will probably start with ID functionality. The new regulations will also commoditize the market as many players try to gain entry and challenge the likes of Infineon, Freescale, Texas Instruments and GE NovaSensor. Contrary to ESP, TPMS is a technically easier challenge that—at least in current generations—is a question of integration of a range of different technologies into a compact low-power system. As a result, many new suppliers including Melexis, Bosch, VTI, Kavlico, and Continental, target the estimated $190 million market expected in 2011 (based on sales of 90 million units). Therefore, some will fall by the wayside.

Sensor Clusters: Currently there appears to be no consensus on how best to integrate disparate sensor elements for no loss in performance or reliability, which requires a full view of architecture. Sensor suppliers like Honeywell and Systron Donner Automotive integrate accelerometers into IMU modules. However, we believe that tier 1 suppliers like Bosch, Denso and Siemens VDO will find this activity easier due to inherent systems-level knowledge. Systron Donner Automotive, which integrates VTI accelerometers into an IMU, could find itself competing with its major customer Continental Automotive at module level. So far, Analog Devices has combined rollover detection and ESP functions (which feature gyros with significant resolution differences) used in TRW's systems employed for SUVs. Bosch is accommodating ESP active safety systems with passive rollover sensing with a new gyro with increased measurement of 240°/s. This ultimately leads to fewer gyroscopes. There is no obvious trend to outsource manufacturing to big CMOS foundries such as TSMC. An exception is the relationship of Freescale with the Dalsa foundry, although this is confined to lower value devices like some types of pressure sensor. Freescale retains in house manufacturing of high-value technologies such as accelerometers and gyroscopes. In some cases, MEMS foundries could play a role after

acquisitions or restructuring or new products needing 8" fabs. One such foundry betting on automotive is Silex. Also tMt is currently cooperating with a well-known automotive MEMS manufacturer wanting 8" for a new product, though most others look to higher volume CE opportunities. The automotive sensor market will prove too tough for many startups or consumer-market oriented companies looking to enter this space. Opportunities will exist but largely for non-safety critical sensors used in GPS navigation or infrared sensors. STMicroelectronics is an exception, leveraging strong connections in the industry through its existing IC business. We know that several suppliers of ASIC to the automotive market are also looking at widening their offering to include sensors. Source: Wicht Technologie Consulting



Graphene p-n Junctions - The US is the first to have created a locally-gated p-n junction in graphene - a 2D sheet of carbon just one atom thick. The charge density in the device is controlled by applying voltages to electrodes that are attached to the surface of the material. The fabrication technique could open the possibility of graphene transistors that could be much smaller and more efficient than today's silicon-based devices. Graphene might form a p-n junction, a basic building block of a transistor, by placing positive and negative electrodes next to the surface of graphene. The positive electrode would attract electrons to the region of graphene below it, creating an area of excess negative charge (an n-type semiconductor). Similarly, the negative electrode repels electrons and creates an area of excess positive charge (a p-type semiconductor). But it's not easy to place a tiny metal electrode (or local gate) very near to the surface of graphene without damaging the graphene or changing its electrical properties. One obvious solution is to first deposit a very thin insulating layer on the graphene followed by the metal electrode, but it has proved hard to find an insulating material that will form an extremely thin and well-ordered layer on graphene. Harvard University used atomic layer deposition (ALD) to create a suitable insulating layer by depositing successive layers of nitrogen oxide, trimethylaluminium, and aluminum oxide onto graphene. A metal electrode of titanium and gold was then deposited on top of the insulator. The technique was borrowed from chemists who had developed it to coat carbon nanotubes, which are essentially graphene sheets rolled up into tubes. The graphene sheet itself rests on a silicon substrate coated with an insulating layer of silicon oxide. The silicon acted as the second electrode controlling the p-n junction. The researchers measured the resistance of the graphene as a function of the voltages applied to the electrodes and confirmed that the graphene contained p-type and n-type regions. But unlike other semiconductor materials, this device had no energy gap and this means that the junction could not be used in a practical transistor to switch electrical currents***. [But if CNTs, essentially cylindrical graphene that is commercially available, can make reasonably good transistors, why does graphene really offer?]***



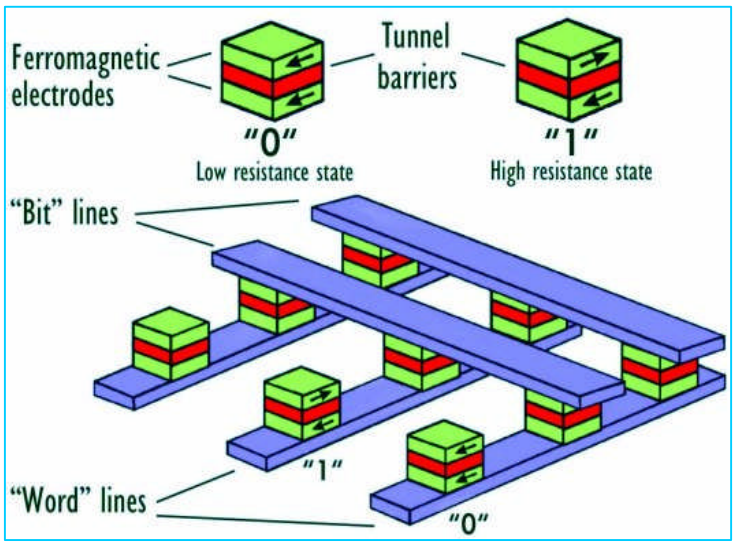
Inorganic Nanotubes - Georgia Tech (GIT) has defined a new class of inorganic nanotube materials that are analogous to volcanically formed minerals found in Japan and New Zealand. By combining aluminum oxide with silicon and germanium, the group at Georgia Tech claims to have defined a new class of single-walled nanotube that is less expensive to fabricate than carbon nanotubes, offering properties that are easier to control. [Other inorganic nanotubes are known]. Inorganic metal oxide nanotubes are closer to what the chip industry is already fabricating. The metal oxide nanotubes can be formed at normal atmospheric pressure below 100°C. Other groups are working on planar metal oxide devices by which heterojunctions are created by confining two types of insulators between two different types of metals. But GIT believes that their metal-oxide nanotubes could someday be similarly sandwiched between metals to craft a new class of nanoscale metal-insulator electronic devices.

The inorganic nanotubes are formed by starting with aluminum and attaching atoms that have different bond lengths, like silicon or germanium, and this causes curvature that forms them into tubes. Because the nanotubes are synthesized in dilute solutions of water, aluminum, silicon and germanium, the varieties of inorganic nanotubes that can be formed in this manner are theoretically endless, depending on the precise mixture of elements, their temperature, pH and similar easily controlled process parameters. The metal oxide materials are very easy to control because of the mild chemistry used, but reactions can take days to complete. So far the two nanotube materials fabricated are varieties of aluminosilicogermanate (AlSiGeO) with diameters of from 1.5 to 4.8-nm and lengths of less than 100-nm. Electronic characterization of the current experimental material reveals band gaps between 3.5 to 4.5 electron volts, making them similar to gallium nitride and zinc sulfide. GIT plans to lower the band gap in the next generation of materials by inserting transition atoms into the organic nanotube to bring them nearer to traditional semiconductors. The researchers also plan to do detailed characterization of the metal oxide nanotubes, examining their electronic properties as well as chemical properties such as adsorption and diffusion. The team further wants to create a general theory regarding the formation of the materials, along with detailed models, so that new versions can be designed with specific desirable properties. Source: EE Times.

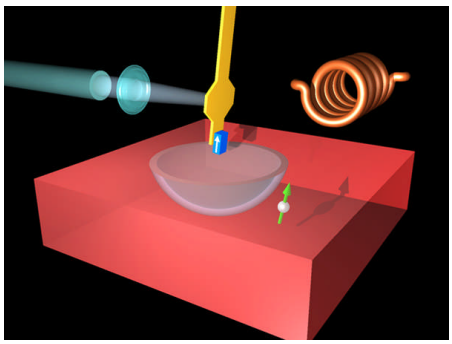
TECHNOLOGY FOREFRONT

The Future Solid Memory Transition - Sooner or later, the electronic charge will be replaced as the storage entity. Unlike logic devices that rely on electronic transistors, there are many ways to store information. We've been using mechanical (since Edison's time), magnetic and photonic modes for decades. Solid-state is getting ready to move to magnetic, thanks to IBM's fundamental discovers in physics; most disk drives use IBM discovers. Now, IBM and TDK are cooperating to advance RAM technologies, announcing the launch of a new research program aimed at MRAM; Magnetic Random Access Memory. MRAM appears to have the potential to create much more compact memory than e-storage. It has been in development for a long time, but has seen little actual use. IBM's announcement comes as no surprise, as they have been pushing for and

pioneering MRAM development for a long time now. IBM claims both them and TDK will be able to work together to explore more versatile uses of MRAM technology. The companies will leverage their respective expertise in areas of fundamental research for new memory technology and magnetic device development to create a high density, high capacity MRAM integrated circuit which can be used as standalone memory or embedded into other IC solutions. MRAM promises a lot of advantages over existing DRAM technologies, such as vastly lower power draw and increased speeds, but is currently plagued by size and cost issues. It has been named in the past, by companies like IBM, as a potential successor to all forms of existing RAM technology. Perhaps with TDK's assistance they will be able to push that agenda further. Source: IBM's site.



Beyond Silicon - ***[IBM is leading the way in "blue sky" R&D in many fields. They seem to be doing a considerable amount of single-atom electronics and memory storage work].*** IBM's Zurich Research Lab has demonstrated a molecular switch that could replace current silicon-based chip technology with processors so small that a supercomputer could fit on a chip the size of a speck of dust. IBM now claims its molecular switch could replace today's semiconductors with devices smaller than those called for by the International Technology Roadmap for Semiconductors while exceeding the theoretical capabilities of CMOS chips. The wavelength of an electron is about 10 nm so you can't shrink semiconductors down to the size of single atoms that are only about 1 angstrom. If you want to perform computations or data transmission at the atomic scale, you have to find an alternative to semiconductors and that's what the Zurich lab is doing; jumping ahead to design a new building block for molecular-sized circuits that could completely replace both silicon circuitry and copper wiring. Source: EE Times.



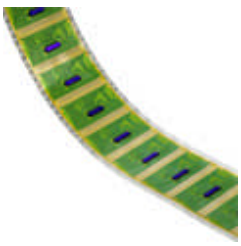
PACKAGING

TSMC Boosts WLP - Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) will spend about $60-million on capital to establish 300-mm, wafer-level packaging (WLP) technology. The funds will also be used for WLP capacity to meet future market demand.

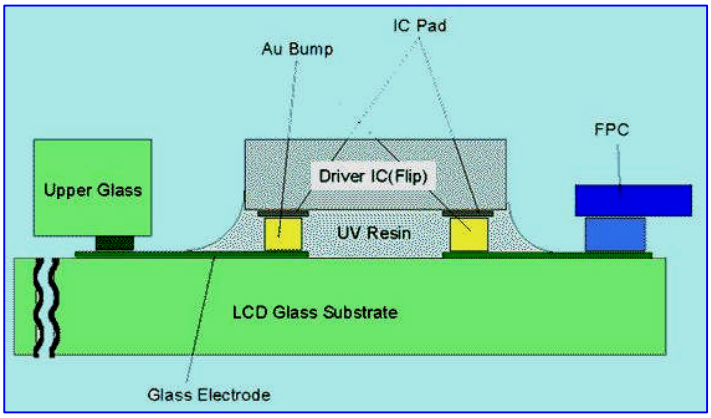
TSMC (Hsinchu) is the world's largest silicon foundry provider. TSMC did not elaborate, but the company has been developing packaging technology over the last several years. The company has limited internal production, but it mainly works with subcontractors like Advanced Semiconductor Engineering Inc. (ASE) and others. WLP technology can effectively reduce the size of end products and will boost the competitiveness of TSMC. TSMC has also approved capital appropriations totaling $22.8 million for upgrading a monthly capacity of 12,600 8" wafers in 0.18-micron logic process to 11,100 eight-inch wafers capable of high voltage, radio frequency (RF), and BiCMOS processes. Source: EE Times.

Freescale's RCP - The new package eliminates wire bonds, package substrates and flip-chip bump interconnects [***but it sure looks like the GE Chip-First idea from the 1990's***]. It is supposed to reduce die area and thickness by 30% compared with standard molded-array plastic ball grid array. Freescale introduced RCP in July 2006, and has now spent a year honing the technology and demonstrating it in applications. The reliability and durability specifications RCP has recently passed include MSL level 3 with 260°C reflow testing, 1500 cycles of air-to-air thermal cycling after preconditioning, and 96 hours of unbiased, highly accelerated stress test (HAST) after preconditioning. The industry is also currently trying to solve problems related to lead-free solutions and the stresses associated with bonding to these materials. Freescale decided to move RCP in a direction in which they could find a compatible material set that would solve many of the problems with current and future generations. RCP meets RoHS requirements; it is a lead- and halogen-free technology and is extendable across more than one platform or application. RCP is a chip-first technology that eliminates the substrates presently used for die mounting and wire bonding or flip-chip. The package is built around the assembly or die. The material sets are said to be very compatible with the back end of the silicon process to help remove the stresses. You can do much higher-density interconnects, because RCP technology uses semiconductor processing rather than a standard substrate type of processing that is generally associated with substrates for wire bond or flip-chip. Freescale has also demonstrated embedded components within RCP packages. Source: SI

TCP being displaced by COF in Driver Packaging - Tape-carrier packaging (TCP) is coming under heavy price pressure as it is being quickly replaced by chip-on-film (COF) packaging as the mainstream technology for driver IC packaging amid growing demand for smaller and slimmer consumer electronics. While Chip-on-Film COF (also COG; Chip on Glass) utilization at back-end service suppliers is mostly at 90% or more in the third quarter, TCP suppliers are resorting to pricing in order to keep their capacity running. With LCD panels' resolution increasing, the driver IC pin count is growing and the pitch reducing. Because of its technological limitations for accommodating finer pitch, TCP started to see COF emerge as a replacement mainstream driver IC packaging technology about three years ago. Although Chipbond Technology chairman FJ Wu estimates that in 2006 the industry still saw more TCP capacity than COF capacity, he noted that by the first

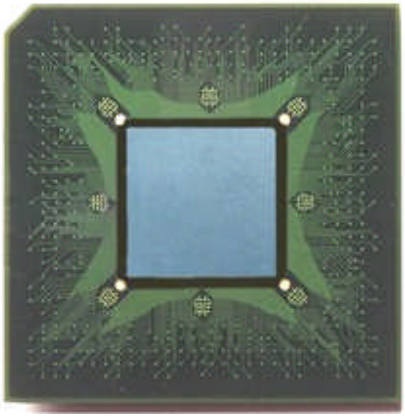


quarter of 2007, TCP had already taken a large lead over COF in terms of the amount of equipment deployed. TCP equipment cannot be adjusted to COF, Chipbond started focusing on COF when purchasing equipment two years ago. However, companies that invested heavily in TCP equipment now face losses when they have to phase out their equipment, the observers added. Currently Chipbond's COF monthly capacity amounts to 34 million units, and will increase to 40 million units by the end of the year, Wu said, adding the company does not have too much pressure from the TCP segment, because it currently only has a monthly TCP capacity of 5 million units. Chipbond's utilization for COF was 80% in the second quarter, and is expected to reach almost 90% for the third quarter, according to the observers. International Semiconductor Technology (IST) was running at 80% for its COF capacity in the second quarter, and it plans to expand its COF capacity 10% to 40 million units in the third quarter, the observers said. ChipMOS' COF capacity is maintaining a 90% utilization rate in the third quarter, and will top 90% in the fourth quarter, the observers added. Source: DigiTimes.



MATERIALS

New Die Attach Films - Henkel is filling out their line of die attach materials and added two new dicing die attach film products, Hysol® QMI5100 and Hysol QMI5200. The film adhesives streamline the die attach process, particularly for stacked die applications. The products are said to combine the properties and functions of die attach film and dicing tape into one product. With these dual structured materials, one need only laminate the film to the backside of the wafer, dice the wafer, pick the die and move to die placement. The films essentially eliminate the need for any dispensing or curing equipment or process steps, as paste dispensing is not required and curing takes place during the standard molding process. The materials enable superior bondline thickness control and eliminate the common bleed issues associated with die attach pastes. Hysol QMI5100 is a 10-micron thick material and is most commonly used on the DAX levels of the die stack. Qualified for use on DA1 (the mother die) and/or DAX, Hysol QMI5200 is available in a thickness of 20-microns. The primary market for Hysol QMI5100 and Hysol QMI5200 is for FLASH and DRAM memory devices. Die placement is said to be fast and with no need for a separate die attach cure. When compared to competitive materials, these dicing die attach films deliver several advantages including minimal or no burring after wafer dicing and extremely fast die placement time down to 0.1 second. Unlike other die attach film materials that require a UV release mechanism, Hysol QMI5100 and Hysol QMI5200 have been formulated as pressure sensitive release materials, eliminating the need for UV equipment and the time associated with a UV release process. Source: Henkel website.



FC Substrate Demand Up - Huge orders from Intel are expected to give a strong boost to Taiwan's flip-chip substrate manufacturers in the fourth quarter of this year. Intel is struggling to fill a flood of demand for its products. Following price cuts of 50% on its Core 2 Quad Q6000 CPUs and other reductions on Conroe and Kentsfild CPUs, Intel has experienced a major increase in demand for those products. In addition, demand is expected to soar in the mid-August back-to-school season and the upcoming shopping season that will begin in October. Intel is outsourcing the production of huge amounts of the flip-chip substrates it needs for its CPUs and chipsets. Some independent chipset makers, such as the NVIDIA Corp., VIA Technology Inc., and Silicon Integrated Systems Corp., are following Intel's lead in placing increased orders for the substrates. Intel currently sources its substrates from the Ibiden Co., Sinko Electronic Industries Co., and NGK Spark Plug Co. of Japan, as well as the Nan Ya PCB Corp. of Taiwan. With the explosive growth in orders, however, the production lines of these manufacturers are fully booked and the supply of substrates has become tight. Now Intel takes about 60% of the total global supply of flip-chip substrates. Makers of chipsets supply about 25-30% of this amount, with suppliers of systems-on-a-chip accounting for the rest. The other leading CPU supplier, Advanced Micro Devices Inc. (AMD), does not affect the market for flip-chip substrates very much because it uses mainly ceramic substrates. The tight-supply situation is likely to get worse, as Intel plans to launch mass production using its new 45-nanometer process in the second half of this year and to introduce 15 new CPU models in the fourth quarter. Another supply-and-demand factor is Intel's planned switch of specification for its flip-chip substrates from X64 to X66, requiring additional layers of processing and 30-40% more production capacity. Taiwan's Nan Ya PCB Corp. will obviously benefit from these developments. The company has already boosted the utilization rate of its production lines to 100%, and is poised to report record revenues in August. In fact, Nan Ya has been forced to pass some orders for chipsets, graphic cards, and system-on-a-chip applications to other Taiwanese makers of substrates, such as the Phoenix Precision Technology Corp. and Kinsus Interconnect Technology Corp. Source: CENS.

EQUIPMENT

TSV must be Real - [Everyone is talking about directly stacked and connected chips for 3D. But some, mostly the chip and wire packaging people, say it's not going to happen. But when the semiconductor equipment companies offer TSV systems, and that's a strong endorsement for viability]. Lam Research, just announced the first equipment for 300-mm 3-D IC through-silicon via (TSV) etching. The Syndion 2300 etch system is expected to be in production during the first half of 2008. The company said that it had been developing the technology for over two years. They believe that they are the first supplier to ship a 300mm system for TSV etch applications. The results are from leveraging their extensive 300-mm and MEMS deep silicon etch production experience.

Customers are said to be at the early stages of developing the technologies that will cost-effectively enable interconnects for die-to-die and wafer-to-wafer stacking over conventional wire-bonding technologies. Lam Research stated that it had been able to create etched vias ranging from 2 to 100 microns wide with depths of 20 microns to greater than 400 microns, while maintaining customers' required profiles. The Syndion system is built on Lam's 2300 platform that can be configured for both 200mm and 300mm wafers and uses its patented high-density TCP planar plasma source. ***[What's important here is that MEMS does not use 300-mm since its way to big. But all of the memory fabs use 300-mm and they're the ones who want to stack].***