SEMICON, PACKAGING & ASSEMBLY REPORT
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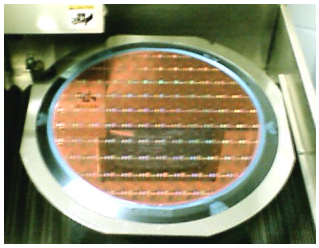
ET TRENDS

BUSINESS NEWS

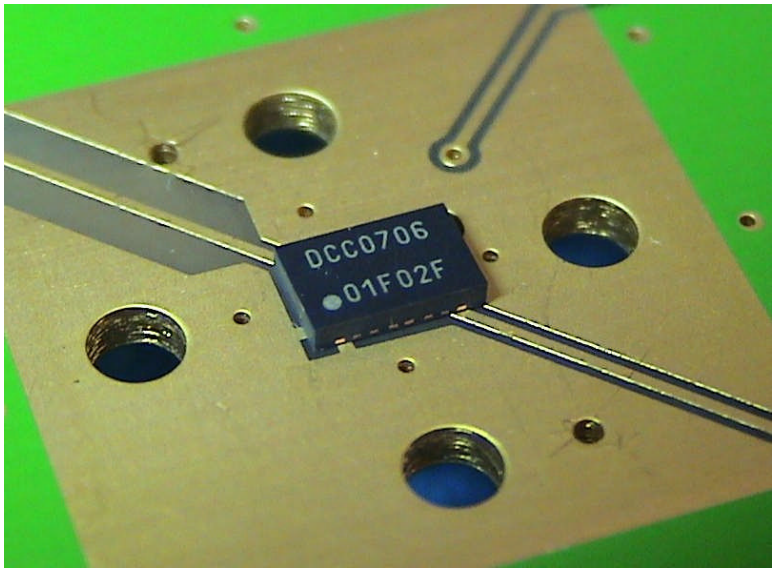
Chipbond to Build 12,000/Month 12-inch Solder Bumping Plant - Chipbond Technology is the largest gold bumping service provider in Taiwan. The company plans to build solder bumping facilities to process 10,000-12,000 12-inch wafers monthly. The company will issue a total $60.5-million worth of convertible bonds over 5-years to pay back loans and purchase equipment to develop 12-inch solder bumping. The company is utilizing its five years of experience in 8-inch solder bumping for the development of the 12-inch service. Solder bumping currently accounts for about 5% of the company's revenues. While its gold bumping capacity is 180,000 wafers a month, mostly for LCD driver ICs, Chipbond is hoping to diversify risks after seeing big fluctuations in the TFT LCD market in recent years. Solder bumping service at 12-inch is expected to boost the company's revenues and profits, as the average selling prices for 12-inch solder bumping are over $200 each wafer, much higher than the current $80 for an 8-inch wafer. Gold bumping utilization at Chipbond and International Semiconductor Technology (IST) was at 70% each in the fourth quarter 2006.



China-Intel Fab - China has approved plans by Intel, the US semiconductor company, to build a $2.5-billion advanced chip fabrication plant in the northeastern city of Dalian. The plant would be a breakthrough for China's efforts to build a strong semiconductor sector, but is likely to cause concerns in the US about the transfer of strategic manufacturing technology to a potential economic and military rival [a communist country]. China's National Development and Reform Commission said it had given the US company approval to build a wholly owned plant in the port city that would produce chipsets for computer central processing units, or CPUs. The plant would be able to produce chipsets with details as fine as 90-nm across on 300-mm silicon wafers. The Dalian plant would considerably increase Intel's commitment to China, where it has already invested $1.3-nbillion and employs 7,000 local staff. Intel already has relatively low-tech chip assembly and test facilities in Shanghai and the western city of Chengdu. China's leading chipmakers are all foreign-owned but no company with Intel's global presence has previously made the country a manufacturing base. The Dalian plant is likely to be Intel's biggest single investment in Asia, a region that represents the fastest growing and largest geographic segment for the company. [Many of us don't see the rationale in this decision. Fabs have low labor content and the greatest cost is power. Wafers have high value per weight, so shipping cost is a non-issue.]

MEMS & BIO-CHIPS

MEMS Timing IC Chip - A strategic Alliance between **Discera** Inc. and **Vectron** International has led to the introduction of the first MEMS-based CMOS timing circuit that can directly replace traditional quartz crystal oscillators. The chip can replace FBAR (Film Bulk Acoustic Resonator) and SAW (Surface Acoustic-Wave) timing devices. *[What are the die attach requirements?]*. The MOS1 family of MEMS oscillators delivers high performance and low cost in a small form-factor to address a wide variety of consumer and some military applications. It includes a MEMS resonator, and is a fabless design wire-bonded to a signal-conditioning ASIC using wafer-level processing (WLP). The MOS1 is a drop-in replacement for existing timing devices on the market. It's ideal for camcorders, still cameras, MP3 players, DVD players, mini disk drives, PDAs, TV players, set-top boxes, etc. The four versions in the MOS1 family generate frequencies ranging from 1 MHz to 125 MHz with a choice of frequency tolerance and stability figures of ±100 ppm, ±50 and, ±20 ppm over an operating-temperature range of –40°C to 85°C. They all consume less than 1-µA of standby current, an extremely important parameter for consumer electronics items like mobile phones and other portable products. All of Discera's oscillators are specified to age at a rate of ±5 ppm/year or less, and are available in either plastic quad no-lead (QFN) or ceramic packages, with dimensions of 3.2 x 5 x 0.85 mm (QFN) or 1 mm (ceramic). Discera is touting lower costs, shorter lead times, and better reliability. The cost to enter the MEMS oscillator market is less than one-half of that for a quartz oscillator and the company sees a 15% per year cost reduction for CMOS MEMS devices. MEMS oscillators also provide a unique manner in defining an operating frequency over a wide range with high resolutions up to 2 ppm.



ST-Micro & MEMS - Nintendo's Wii is the hottest computer game has two wireless remote controls that track any movement encouraging players to engage opponents to be more active and competitive. The detecting motion is critical to the success and depends on a $3 MEMS chip. STMicroelectronics, the chip supplier, got into the MEMS business a decade ago in order keep an obsolescent chip-making plant running. *[MEMS can use older fabs since extremely fine features are not required]*.

Background: ST-Micro's chief MEMS designer Vigna, went to the University of California-Berkeley to study MEMS and do some work-study stints at local companies. Then, ST assigned him a staff, and invested heavily in their MEMS research. In 2001, 3-years into the project, Vigna hit on the ideal mass-market product: a chip that could detect motion in 3-dimensions. There were already tiny, cheap MEMS devices that could detect motion in two dimensions (2-axis accelerometers). Motion detection can use a device called an accelerometer; a cantilever hewn from silicon and teetering between two electrodes. Apply a 1-volt field, and the cantilever's beam will vibrate; accelerate the package, either by pushing it in one dimension or by rotating it, and the beam's tip will trace an ellipse. The eccentricity of the ellipse measures acceleration. Place two such accelerometers at right angles, and you can track acceleration in a plane, add a third, and you can track it in space. ST's earliest device occupied a cubic inch, a lot smaller than the brick-size gizmos in aircraft, but still way too big for a consumer product.

So ST set about shrinking chips to keep costs down and found a way to package the MEMS chip in plastic rather than in expensive ceramic. One of the first applications of the 3-D sensor was in laptops, where sensors guard against damage from a fall. In the split second of free fall that comes before the collision with the floor, the sensor tells a controller to park the read/write head safely away from the hard drive. Another application came in 2003, in a Maytag washing machine that uses a somewhat smaller sensor, 14 mm x 7 mm x 4 mm, to detect vibrations due to an unbalanced load and to adjust the washer's speed to dampen them. Another ST product enables the user of a cellphone or a PDA to adjust the display of images or retrieve data from memory by just tilting the device. Games were already on Vigna's to-do list when he discovered that Nintendo, in Kyoto, was ahead of him.

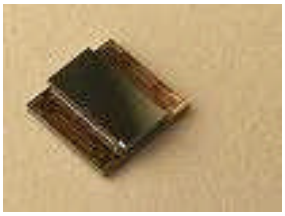
Vigna met **Nintendo** in March of 2005 and both company visions were in line. Two months later, ST delivered a prototype sensor, and 16 months after that, Nintendo launched worldwide sales. Since then, the demand for the game has strained production. Vigna says the Wii has been the biggest application of all "because the MEMS chip is the core of the product." In recognition of his work, ST recently made Vigna the general manager of its MEMS product division. That means he has to plan for the long term. First, he wants to make the sensor even smaller, even cheaper and tougher. "I want it to fit in all kinds of places; shoes and textiles, for instance, where it might be useful for medical monitoring". Then he wants to make a three-dimensional gyroscope, to measure rotation around 3 different axes. Today, such products are quite big, a cube 10 centimeters on a side. "We want to do this in less than a 30-millimeter cube, to serve as an image stabilizer in cameras and to track a person's position in the intervals when he can't get a GPS signal." Better still, he adds, would be to throw in a magnetic detector, freeing the navigator from GPS altogether. It would be yet another marvel from Lilliput—the smallest compass ever sold.

Flow Sensor - Omron has the first flow sensor to use thermopile technology that converts thermal energy into electrical energy. This is said to be more accurately and efficiently measure air/gas flow speed in medical applications. The D6F series of MEMS flow sensors measure flow speed from 1 mm/s to 40 m/s. This new thermopile method is said to deliver a variety of advantages including low-cost implementation, low-power consumption, accurate measurement and high sensitivity. In comparison, conventional flow sensors use a resistance measurement method by tracking the electrical resistance change of a material due to changes in temperature. This method requires a labor-intensive adjustment of the resistance balance, said the company. The D6F, which measures 15 x 20 x 60 mm, operates over the temperature range of -10°C to +60°C with a supply voltage of 12 to 24 Vdc while consuming only 15 mA. It features an integral orifice with an analog output of 1 to 5 Vdc. Applications include oxygen concentrators, inhaled anesthetics, heliox, CPAP, and ventilator applications.

Hitachi/Takara Bio Virus Detection System - Hitachi, Ltd. has developed compact automatic virus detection system jointly with Takara Bio. The system comprises Hitachi's proprietary virus collection system and virus genes analyzer, developed based on Takara Bio's ICAN (Isothermal and Chimeric P- rimer-Initiated Amplification of Nucleic Acids) method. Equipped with two MEMS chips, the system saves significantly virus collection and analysis processes, which used to require a week or so, so making the total system fit within 50x45 cm. Setting the MEMS chips, which concentrate and collect virus through the collector, inside the analyzer allows for detection of the virus genes in 40 to 120 minutes. After the process, only the chips need disposing of, which helps reduce examiners' chance to be virus-affected. Hitachi expects the portable system to meet on-spot virus detection needs at care facilities for the elderly, food processing factories, airports and seaports. It aims for sales - of total 10 billion yen for the next three years.

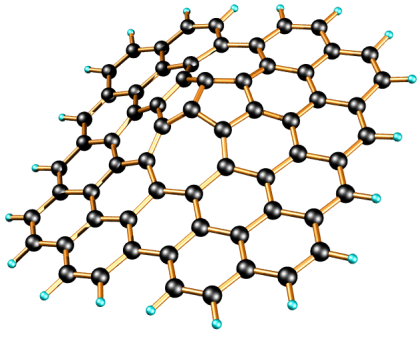
MEMS Motion Stabilizers - **InvenSense** has created a MEMS-based gyroscope for camera phones that will begin shipping later this year. The tiny micromachines react to and counteract vibrations in a user's hand, steadying the camera phone's lens. InvenSense's "Gyroscope" was created to fit within the tiny confines of a cellular phone, which is taking on the functions, and feature sets, of low-end dedicated cameras. InvenSense has already received purchase orders and is working with key customers. The company's manufacturing contracts call for a million units per month to be produced. Motion sensing gained notoriety with the introduction of Nintendo's Wii game console, whose controller senses motion and uses it to control the action of objects on screen [see previous]. Sony, in a surprise, developed a similar concept and showed off the technology at the recent E3 show in Los Angeles.

For InvenSense's Gyroscope, however, it's the involuntary motion of the hand that must be sensed and eliminated, not deliberate gestures. Camera blurriness occurs jitters it up and down, due to involuntary muscle movement. The human had vibrates at about 10 to 20 times per second (10-20 Hertz) and requires a gyroscopic sensor capable of sensing 150 Hertz to be able to detect and filter out the noise of the moving hand. Every camera maker in Japan that makes a point-and-shoot camera includes image stabilization. Cameras use a relatively large but effective piezoelectric gyroscopes filter out the hand jitter. Cellular phones, however, have used cheaper consumer versions that aren't sensitive enough to filter out the noise. In that case, cameras often ratchet down the resolution to allow a relatively sharp image, turning a 3-Mpixel camera phone into a 1-Mpixel clunker. Normally, the image is stabilized in one of two ways. Optical stabilization, the more expensive option, "floats" the entire sensor housing within the camera, stabilizing it, and allows users to shoot images at a slower exposure than normal. Electronic image stabilization uses the controller chip's software to fix the image. In video, one frame is compared against the next. Within a still image camera, the camera first takes a fast image, designed to establish the edges of objects, than a longer shot that captures the color information. The two shots are then composited together by the camera's processor. Since the stabilization is calculated, camera makers and smart phone makers can save money and die space by choosing this route. Cellular phone manufacturers are asking for sensors that cost about a dollar per axis of sensitivity. InvenSense's Gyroscope measures 3.5 millimeters on a side, and the die will be reduced to a 3-mm x 3-mm square within the next revision. The design also allows the processor to be placed close to the sensor itself, reducing the noise and power needed to transmit the information across the camera housing.



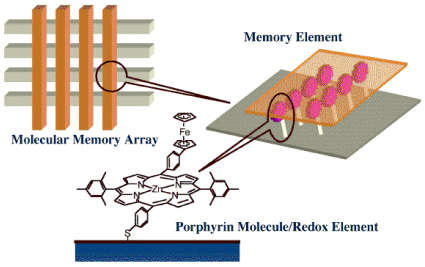
TECHNOLOGY FOREFRONT

MANCHESTER **Nanoelectronics** - Researchers have used graphene sheet to create the world's smallest transistor. The **University of Manchester** has revealed details of transistors that are only one atom thick and less than 50 atoms wide. Two 2 years ago, the researchers discovered a new class of materials that can be viewed as individual atomic planes pulled out of bulk crystals. These one-atom-thick materials, and particularly graphene, un-rolled carbon nano-tubes, have rapidly become one of the hottest topics in physics. The first graphene-based transistor was reported by The University of Manchester team at the same time as the discovery of graphene, and other groups have recently reproduced the result. But these graphene transistors were very 'leaky', which has limited possible applications and ruled out important ones, such as their use in computer chips and other electronic circuits with a high density of transistors. But graphene remains highly stable and conductive even when it is cut into strips of only a few nanometers wide. All other known materials, including silicon, oxidize,



decompose and become unstable at sizes tens times larger. This poor stability of these materials has been the fundamental barrier to their use in future electronic devices – and this has threatened to limit the future development of microelectronics. But the group now has made ribbons only a few nanometers wide and cannot rule out the possibility of confining graphene even further, down to maybe a single ring of carbon atoms. The research team suggests that future electronic circuits can be carved out of a single graphene sheet. Such circuits would include the central element or "quantum dot", semitransparent barriers to control movements of individual electrons, interconnects and logic gates – all made entirely of graphene. The team has proved this idea by making a number of single-electron-transistor devices that work under ambient conditions and show a high-quality transistor action. No technology can cut individual elements with nanometer precision and they have to rely on chance by narrowing our ribbons to a few nanometers in width; some were too wide and did not work properly whereas others were over-cut and broken. The does not expect that graphene-based circuits will come of age before 2025; until then, silicon technology should remain dominant.

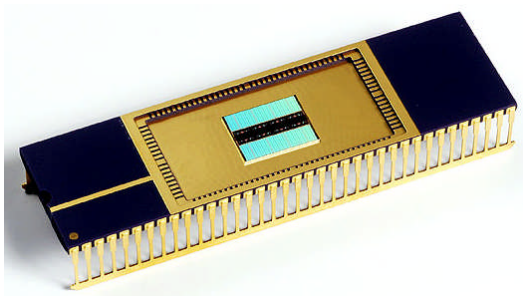
New Memory Sooner or Later - Memory cells contain circuits etched at a width of 50 nanometers. But makers of memory chips are looking ahead to a day, not too far off, when technology based on silicon hits the laws of physics and memory can't be made any smaller. You get into the 25-nm scale and there may need to be a new structure for nonvolatile memory, and 25nm is not that far away, but the big challenge is only a few generations. While CPUs have circuits that act as pipes that guide streams of electrons, memory chips use pools of charged electrons to store data, and it gets harder to read the data as the number of electrons in each pool shrinks. The possible alternatives sound like science fiction: M-RAM, P-RAM, molecular memory and carbon nanotubes. In the next decade, we're going to need some significant new technologies, according to Micron. P-RAM, or phase-change memory, is one of the most promising new technologies is in which the physical state of a germanium alloy is changed between crystalline and amorphous to store data. IBM has developed a prototype chip that performed 500 times faster than current flash memory while using less than half the power.



The technology can be used to create circuits as small as 20-nm, less than half the size of current cutting-edge flash technology. Other promising new technologies include magnetic memories that use magnetic fields instead of electrical charge, polymers or custom-designed molecules whose electrons can be easily manipulated, and carbon nanotubes. The challenge researchers face with most of those technologies is finding a way to make them cheaply in large quantities. New technologies will likely be cross-licensed throughout the industry, which is now dominated by five companies that account for more than 80% of the total output. The five next-largest vendors account for all but 1% of the remaining output. New memory technologies will all have to meet several key requirements. For example, they will have to be able to store a lot of data, read and write that data quickly, and be able to retain that data when the power is switched off. Perhaps

most crucially, it will have to be possible to produce them using current manufacturing techniques. If not, they will have to be so attractive that companies will be willing to spend heavily on all-new factories. All these different memory technologies hold a lot of promise, but the cost of implementation will be enormous.

The Phase Memory Phase-In - Intel is preparing to sample a 90-nm 128-Mbit phase change memory to customers in the first half of 2007 with mass production before the end of 2007. The memory is a drop-in replacement for NOR flash non-volatile memory although its performance characteristics means it could be used it a greater range of applications and come to replace in DRAM in some systems. Intel has been a licensee of chalcogenide-based phase change memory technology from Ovonyx. Intel has been actively researching the technology for 6 years even though Ovonyx has been touting the technology, without commercial success, for more than 30 years. Intel and STMicroelectronics had teamed up their research on chalcogenide-based phase-change memory as a likely successor to flash as a non-volatile memory, in June 2006. Interest in phase-change and other non-volatile memory technologies has increased markedly in the last five or six years as there are increasing concerns that flash memory may struggle to scale. Qimonda AG, formerly the memory operation of Infineon Technologies AG, is researching phase-change memory technology with IBM Corp. and Macronix of Hsinchu, Taiwan. Intel's 128-Mbit phase-change memory had demonstrated 100 million read-write cycles of endurance and a capability for much greater than 10 years data retention.



MATERIALS

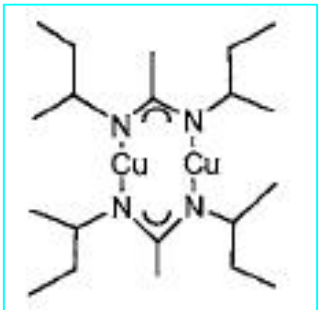
Micron Washington University Silicon Materials Lab - The new lab will research new combinations of materials for use in semiconductor manufacturing. The industry is facing the larger challenges as chips get smaller and are reaching a physical limit with nano-scale effects changing material behavior. The Department of Materials Science & Engineering and Micron will focus the new Micron Laboratory at the Seattle-based university and focus around silicon that is still a good material for the active area of a chip, where the electrons travel, but the supporting material will have to change as the technical limit is pushed. Smaller devices will require new combinations of materials. The first goal for the University of Washington's Micron Laboratory for *Combinatorial Materials Exploration* is to finding these new combinations of materials. Micron and its Micron Foundation will provide the lab with more than $400,000 in equipment and $500,000 in cash, in order to allow collaborative research leading to faster, more efficient and cost-effective screening of new materials. Today's silicon-based transistors are predicted to be obsolete by 2025. New materials will be required to combine optical and magnetic signals on future microchips and be compatible with

existing silicon electronics. Now, many possible successors are vying for favor. Testing them all quickly is beyond the ability of conventional materials testing.

Micron Lab's equipment will automate materials testing by creating a wafer, called a materials library, whose properties change gradually. By layering these wafers, a single test can evaluate all possible combinations of important factors, such as manufacturing process, material composition and atomic structure, to see which produce the best attributes. Similar techniques for screening candidates have long been used in the pharmaceutical industry, but are only beginning to be used in materials research. The new lab will work cooperatively with other institutions using combinatorial materials testing, including the National Institute of Materials Science in Japan, the Pacific Northwest National Laboratory in Richland, WA, and the University of Maryland in College Park. Materials scientists predict that the abundance of data generated by this type of screening will have the same effect on their field that the Human Genome Project had on biology.

The lab will be directed by a multidisciplinary team of 5 UW faculty members. Physicist Marjorie Olmstead will help assess why materials respond in certain ways; materials scientist Raj Bordia will study whether combinations are compatible and stable; electrical engineers Bruce Darling and Scott Dunham will conduct modeling experiments and build prototype devices. The fast pace of today's computer industry means research once carried out in many steps, Ohuchi said, is now being done simultaneously. All results will be collected in a publicly-accessible computer database, and while the initial motivation for the lab is to test semiconductors for the computer industry, over time it may be used to test new materials for energy and environmental uses, such as components for solar cells and fuel cells, or to discover replacements for dwindling resources, such as the indium used in flat-panel display screens, Ohuchi predicts (EDN report).

Rohm & Haas licenses **Harvard** Materials - The company's Electronic Materials Division has licensed a novel class of metal amidinate compounds for making thin films of metals and metal compounds by atomic layer deposition. Rohm and Haas has exclusive rights to manufacture and market the amidinate compounds to semiconductor manufacturers. Atomic layer deposition (ALD) is a technique for making thin films that deposits a single layer at a time with the thickness of only one atom and is meant to provide exceptional control of the thickness of the thin film. Rohm and Haas says it will produce these compounds at its North Andover, MA facility and will collaborate with Harvard scientists to further develop this technology for advanced atomic layer deposition and chemical vapor deposition (CVD) processes. The amidinates developed by Harvard are believed to be ideally suited for advanced high-k dielectric, metal gate and barrier/adhesion layers and should provide manufacturers with improved functionality, throughput and thermal stability. Several large semiconductor manufacturers have already started to develop material integration schemes using ALD and CVD processes.



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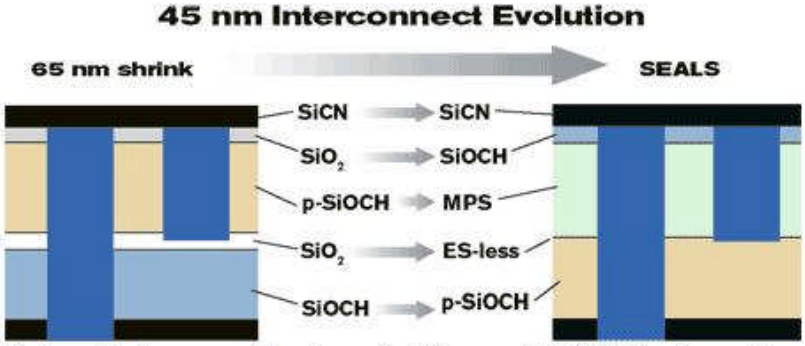
2007 IEEE International Interconnect Technology Conference

The 2007 IEEE International Interconnect Technology Conference (June 4–6, 2007) provided pre-prints for the theme of how "new" materials. Semiconductor materials being explored include ruthenium, rhodium, manganese and carbon nanotubes (CNTs). Fujitsu will report on nano-clustering silica used to build a full interconnect structure with a good total effective k (keff) value. That combined with an ultra thin barrier metal resulted in RC delays 86% less than what's listed in the 2006 International Technology Roadmap for Semiconductors (ITRS) update. NEC demonstrated the practicality of replacing tungsten with ruthenium as a liner/barrier. The advantage of ruthenium is that it can be plated on directly, eliminating the need for a copper seed layer, but critics have said it is neither a particularly good barrier nor seed layer. NEC's changed the grain structure of the ruthenium so that its orientation was more compatible with copper, leading to less electron scattering along the sidewall. Rhodium was shown to have good qualities for void-free filling of high-aspect-ratio structures at the contact level, where tungsten is still now commonly used. IBM (East Fishkill, N.Y.) demonstrated that using a physical vapor deposition (PVD) titanium/atomic layer deposition ruthenium/electroplated stack for the liner/seed/fill results in an overall resistance that is twice as low compared to chemical vapor deposition using tungsten and slightly lower than copper fill stacks. In addition, the ability to use a thinner liner layer than that used for a copper-base fill process provides a greater potential for extendibility of rhodium fill into future CMOS. Sony researchers have also explored the advantages of another manganese. Their method combines copper/ultralow-k interconnects with a self-formed manganese oxide (MnOx) barrier layer that was shown to have lower resistance and higher reliability than copper alloys. They concluded that this self-formed barrier process is the most feasible technology for 32-nm node copper/ultralow-k interconnects. NEC is also evaluating new metals and porous dielectrics.

The SEALS structure replaced all films, except the SiCN capping layer, with lower k value dielectrics. The NEC conference paper describes the chip-to-package interaction related to the SEALS interconnects. In addition to the wire-bonding reliability, the impact of the coefficient of thermal expansion (CTE) of the epoxy-molding compound (EMC) for the quad flat pack (QFP) and plastic ball grid array (PBGA) package was investigated. They also examined the thickness effects of both the epoxy-molding compound (EMC) and substrate in PBGAs on low-k stack reliability.

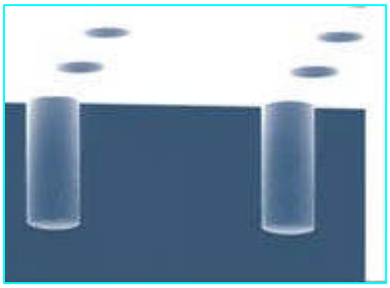


Designed interconnect structures for 45 nm, called SEALS, along with the 65 nm shrink structure.

EQUIPMENT

Applied Materials adds China Development Facility - The company has confirmed reports its first China-based product development facility in the central city of Xi'an. The new Xi'an China Global Development and Technology Support Center is a 106,000-square-foot facility on 25 acres that offers laboratory, tool demonstration and assembly space in its clean rooms. The center is a major expansion of capabilities to help benefit growth throughout China, particularly in the west. The cite is attracting quality employees from local technical universities, and this development and support center will be a cornerstone of our growth strategy throughout China and, indeed, all of Asia. The construction of the Xi'an location could cost Applied as much as $83 million in total.
Applied established itself in China 22 years ago, taking its spot as the first semiconductor equipment company there. Since then, Applied has opened 7 offices located in Beijing, Kunshan, Shanghai, Suzhou, Tianjin, Wuxi and Xi'an, and employs more than 500 people. The facility will perform product development, system localization, engineering, and software support and sourcing throughout Asia-Pacific. The center will also serve as a customer demonstration facility for 200-mm wafer processing and Applied's most advanced metrology and inspection products, the company said. China has been a hot location in recent weeks, with Applied's Santa Clara-based neighbor Intel Corp. also recently making moves there, reportedly receiving the governmental go-ahead for plans to build a $2.5 billion chip plant the northeastern city of Dalian. Applied also noted that it continues to concentrate its volume system manufacturing in Austin, Texas, and the majority of its product development in Silicon Valley.

TSMC and NEXX Systems Collaborate on Cu Plating - NEXX Systems (processing equipment for advanced wafer level packaging applications), announced that it has entered into an ongoing joint development program with Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) of Hsinchu, Taiwan. The program represents a collaborative effort to assess, develop, optimize, manufacture, and/or market electrodeposition processes using the Stratus system, including through silicon vias (TSV), wafer level chip scale packaging, and redistribution layers. In support of this effort, NEXX will both deliver a Stratus 300 automated electrodeposition system to TSMC's Fab 7 in Hsinchu and provide leading process development experts to carry out the development work in conjunction with TSMC's local experts. The Stratus will provide TSMC a proven means of filling TSVs that is cost effective and high yielding. TSMC is creating chip-stacking technologies that enable high performance compact devices.



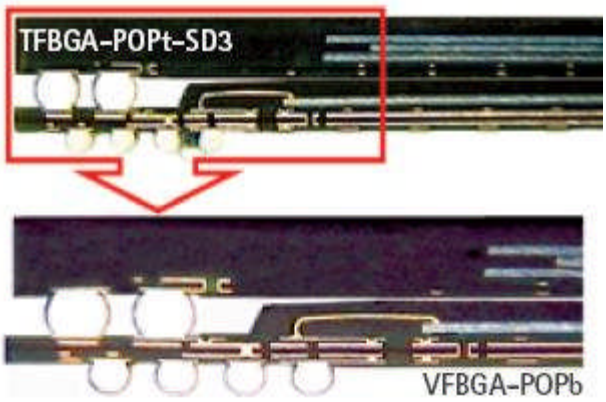
Deep Silicon Etching for 3-D Integration - Through-silicon via etching is used to manufacture MEMS, power devices and, lately, 3-D structures. Three years ago, Sematech cautioned that process and material changes to interconnects would not enable the required performance enhancements in next-generation ICs, and predicted that

the needed boost may come from heterogeneous integration of dissimilar devices. Device manufacturers and packaging houses are looking to wafer-level packaging (WLP) techniques to address the demands of future product miniaturization and increased functionality. 3-D integration is one type of WLP method whereby two or more planar devices are stacked and connected. Multiple approaches in WLP include wire and flip-chip bonding, but a more sophisticated and performance-enhancing, method involves the use of through-wafer vias.

In 2007, the ITRS will incorporate and track the design nodes and architectures for 3-D interconnect for the first time. Through-wafer via technology is being adopted for 3D stacking. Deep silicon etching, based on the Bosch gas switched process, was originally conceived and is still being used for MEMS device fabrication. However, it is also an enabling technology for new ranges of power devices (deeper trenches for higher voltage and current handling) and etching through-silicon vias. The process involves fast switching between silicon etching and polymer deposition for silicon sidewall protection, with SF_6 and C_4F_8 being the principal process gases for etch and deposition cycles, respectively. Benefits include high etch rates and mask selectivities that cannot be achieved by single-step silicon etching. A disadvantage is "scalloping" of the sidewall, an artifact of the etch and deposition cycles that can now be minimized. The growing importance of 3-D packaging has prompted Sematech to develop an industry-wide roadmap to guide 3-D packaging efforts, while IMEC (Leuven, Belgium) is also putting together a consortium with the same end goal. This attention and work will help consolidate the industry effort and promote market acceptance. A range of approaches currently exists, favored by different groups in the IC food chain. Front-end-of-line (FEOL) approaches involve designing in the vias from the onset so that fabrication takes place at the IDM or foundry. The packaging house thins the wafers to reveal the vias and make the IC-to-IC bond. Alternatively, back-end-of-line (BEOL) approaches exist whereby the chip designer leaves exclusion zones for the packaging house to add in the vias. This adds value to the packaging activity, but requires skills currently absent from their conventional activities.

NEW PACKAGES

STATS ChipPAC's fan-in package-on-package - STATS ChipPAC detailed a new fan-in package-on-package (FiPoP) meant to deliver increased functional integration in a smaller form factor, flexibility in stacking conventional memory packages on top, improved final assembly yields, and a lower overall cost as compared to conventional PoP solutions. The FiPoP design is meant



to accommodate multiple die and larger die sizes in a reduced footprint along with the ability to stack off the shelf memory packages with center ball grid array patterns on the top surface, the company noted. PoP is a three dimensional (3D) package in which a fully tested package such as single die FBGA or stacked die FBGA (typically memory die) is stacked on a bottom PoP package which usually contains a logic device or logic device combination (logic plus logic, logic plus analog, etc.). In standard PoP package designs, the top PoP package is interconnected to the bottom PoP package through solder balls around the periphery of the bottom PoP package. Integration of multiple die and larger die sizes in the bottom PoP package has been constrained by the footprint and ball height of the top PoP package. The FiPoP opens up the range of integration options in the bottom PoP package while allowing greater freedom in stacking off the shelf memory packages on top. Fan-in PoP allows the stacking of multiple logic, analog and memory die in the bottom PoP package and accommodates larger die sizes in a reduced footprint as compared to conventional PoP designs, with the structure also allowing for smaller conventional memory packages to be mounted with center ball grid array patterns on top. The fan-in PoP can reduce the final form factor up to 25 % area and have space savings of up to 65 % by volume. One of Fan-in PoP's key features is an exposed array of land pads on the top center surface of the package, instead of a peripheral array around the top of the bottom package substrate as found in a conventional PoP, in order to provide a flexible integration point for memory packages with a center ball grid array pattern.