

Molded Underfill for Flip Chip in Package

Ken Gilleo, Cookson Electronics

Bruce Cotterman and Tian A. Chen, Cookson Semiconductor Packaging Materials
(final, final draft 4.24.00)

Introduction

Flip chip is not only a preferred micro-package, in many cases it is the enabling technology that makes a product possible. There are no practical alternatives for the very high lead count required for modern CPUs. Pentium flip chips have over 2,000 bumps. IBM's latest design that may be used in the world's most powerful super computer, "Blue Gene", will have over 7,000 bumps to connect the 10's of millions of transistors. This is not the realm of wire bonding or Chip Scale Packaging [1]. High density BGAs are also tapping into flip chip for reliability, performance and manufacturing simplicity especially for lead counts above 600. Cost effective reliability with level 3 and higher moisture resistance for flip chip has not been available for flip chip packages until now.

While flip chip bumping and assembly has matured to a large extent, the underfilling process remains an area of intense research and development. The new objective addresses manufacturability and productivity. The industry has responded with the introduction of "*new process underfills*" with the promise of more to come. Pre-dispense underfills, also called "no flows", are being commercialized to improve productivity [2] The no flow underfill (NUF™) strategy appears to fit many of the flip chip on board (FCOB) applications like disk drive and portable communications products [3]. Wafer-Level underfill (WUF™) is also an active area, but success appears to be years away and there are many strategic issues [4]. This article will discuss the newest underfill material and process, one ideally suited to Flip Chip In Package (FCIP), called Molded Underfill (MUF™). This is a new concept pioneered by Cookson in a system approach using Plaskon MUF epoxy mold compound (EMC) specifically designed for flip chip packages. For the first time, flip chip packagers are offered the capability to underfill high I/O flip chips with the productivity equivalent to transfer molding and the reliability found in epoxy mold compounds. But first, let's explore the role that is played by underfill.

Underfill Mechanism

Underfill may be viewed as a specialized encapsulant that fills the gap between chip and substrate to protect the delicate interconnect structure and bare die face. One vital purpose is to mechanically lock these two dissimilar materials together to greatly reduce or even eliminate differential in-plane movement. The underfill simply bonds the low-expansion, high-modulus chip to the higher-expansion, lower-modulus substrate that is typically used with flip chip on organic. The very stiff silicon constrains the X-Y movement of the substrate forcing it to mimic the thermomechanical behavior of the chip. The result is that the two interfaces move in harmony with joint integrity preserved [5].

The ideal underfill encapsulant has a coefficient of thermal expansion (CTE) close to that of the joint. This eliminates stress in the vertical axis that would be produced if the underfill expanded and contracted at a rate substantially different than the chip joints. Most unfilled polymers, including epoxies used for encapsulants and underfills, have CTE values in the range of 70 to 80 ppm/°C. This value is easily brought to an ideal range of 20 to 30 ppm/°C for underfills by adding appropriate inorganic filler. Silica-filled epoxies have long served the packaging industry in the form of solid Epoxy Molding Compounds (EMC) and more recently as liquid underfills. These systems, especially the EMCs, have a long and successful history. Their chemistries are well understood, properties are highly optimized and EMC process makes higher silica content possible. What's more, molding equipment is widely available.

The Underfill Productivity Issue

Many hoped that new *snap flow - snap cure* underfills [6] would alleviate the manufacturing issues. Better capillary flow underfills would break the *bottleneck* so enthusiastically spotlighted by the CSP industry. But did the “snap” underfills break bottlenecks and set records? As it turns out, the fast flowing 5-minute cure state-of-the-art capillary flow underfills still aren't quick enough to wring out cost and aggravation for many products. And these newer materials have reached a performance plateau as they close in on the **laws-of-science** barriers. Yes, the capillary flow products work and they're in production throughout the world, but industry demands real productivity with fewer steps.

Underfilling can be the *epitome of exasperation* from the assembler's point of view. The underfilling process is more than a nuisance, it adds a significant amount of cost when we rigorously analyze productivity. Even a few seconds of added cycle time will translate into a large sum of money at the end of the day - a fortune at the end of the year. The cycle time increase will typically add more cost than the small savings that “no package” can offset. Once again, the underfill material cost is not the core problem – it's rather insignificant, but still high relative to standard epoxy mold compounds. But the underfilling step can increase manufacturing time by 50%, double floor space requirements and add significant dollars in capital equipment. We have estimated that reduced productivity from underfilling may add an extra 1-2 billion dollars per year in reduced output for the industry [7]. But do we really know how best to apply underfill?

Transfer Molding Process

The packaging industry has used transfer molding for decades and this has led to an extensive infrastructure in materials, machines, tooling and general knowledge. The packaging foundries commonly use the transfer molding process to encapsulate all kinds of plastic packages. More recently, the Ball Grid Array (BGA) has become the preferred package for higher lead count. The BGA is now

routinely encapsulated by an efficient transfer molding process using tooling and equipment optimized for this form factor. The BGA transfer molding process is highly efficient, easily automated and produces high quality packages. Figure 1 shows the basic transfer molding machine.

Figure 1 –Transfer Molding Press Diagram

Solid, but reactive filled epoxy mold compound (EMC) in preforms stored at 5°C, is moved to a staging area to achieve ambient temperature. Next, the preforms are transported to storage bins within the automated transfer mold machines. There, the EMC preforms move into the molds and are transferred under pressure into the heated mold section that contains the substrate and assembled chip. The flowed epoxy thermally cures and the mold opens to eject the encapsulated parts. This can be accomplished in single cavities or multiple cavity strips for matrix (flood) molds depending on the size and design of the package. EMC molded underfill performs similar to encapsulants used in transfer molding.

Figure 2 – MUF Solid Underfill Preform

Molded Underfill

Plaskon, an EMC supplier that has targeted the BGA market with low warpage, low stress materials, began developing materials and processes for transfer molding of underfill in the late 1990's. Materials were developed using new micro-particle fillers. The melt viscosity profile was adjusted to maximize flow into the small flip chip gap. Tooling and molding processes were designed that permitted complete filling under the chip. Figure 3 shows a mold cross-section for underfilling.

Figure 3 – Package Mold Cross Section

Extensive development and testing of the process by Cookson and its partner, Hestia Corporation showed that underfilling and overmolding encapsulation could be accomplished in a single step boosting productivity even further. However, tooling can be designed to leave the top (backside) of the chip uncovered if this is required for heat sink contact. Even greater efficiency and versatility is possible by using "area molding", also called "flood molding". Here, an array of substrate containing dozens or even hundreds of flip chips is transfer mold underfilled and the "block" of packages is singulated by sawing. Plaskon MUF goes one step further by curing without the need of a post curing process and equipment.

The Cookson Semiconductor Packaging Materials group, employing Plaskon MUF, has demonstrated complete molded underfilling with various combinations of FC-BGA and FC-CSP packages. Peripheral, as well as partial and full arrays approaching 2000 bumps have been successfully run. These packages have

achieved JEDEC Level 3, 220°C reflow and over 1000 cycles during thermal cycling in extensive reliability testing. The result is flip chip packaging offering lower cost of ownership, the capability to underfill high I/O flip chips with the fast productivity equivalent to transfer molding and higher reliability found in epoxy mold compounds using existing transfer mold equipment in a simple, robust and fast process. Figures 4, 5 and 6 show a scan, X-ray and SEM cross-section of molded underfill parts with no voids.

Figure 4 (scan image)

Figure 5 (X-ray image)

Figure 5 (SEM image)

Conclusions

Flip chip will be the dominant packaging technology for low to high I/O chips, including CPUs and ASICs. The FCIP format will be widely used in the format of the flip chip BGA. While the FC assembly process is fairly well optimized, the underfill step is still a problem that lowers productivity and adds cost. Molded underfill (MUF) appears to be the ideal solution to winning back productivity and maintaining reliability. MUF also is a good fit to the packaging infrastructure that relies so heavily on transfer molding. The MUF process is expected to move into volume production during 2000.

[For further information, contact Bruce Cotterman in Cookson Semiconductor Packaging Materials at 687-624-7386 or bcotterm@cooksonsemi.cookson.com.]

Reference

- [1] Gilleo, K., "Chip Scale or Flip Scale: The Wrong Question?", pp. 30, 31 - 34, Circuits Assembly, Feb. 1998.
- [2] Prevet, M., "No Flow Underfill Reliability is Here – Finally!", pp. P-MT1/1-1 – 1-4, Technical Proc. APEX, Long Beach, CA, Mar 12-16, 2000.
- [3] Johnson, C. D. and Baldwin, D. F., "Pre-Applied Underfills for Low Cost Flip Chip Processing", pp. 73 – 76, International Symposium on Advanced Packaging Materials, Chateau Elan, GA, March 14 – 17, 1999.
- [4] Gilleo, K., and Blumel, D., "Transforming Flip Chip into CSP with Reworkable Wafer-Level Underfill", pp. 159 – 165, Proc. Fourth Annual Pan Pacific Microelectronics Symposium, Kaua'i, HI, Feb. 2 – 5, 1999.
- [5] Gilleo, K. and Blumel, D., "New Generation Underfills Power the 2nd Flip Chip Revolution", pp. 147 – 154, Proc. Pan Pacific Microelectronics Symposium, Mauna Lani, HI, Feb. 10 – 13, 1998.

[6] Gileo, K. and Blumel, D., "The Great Underfill Race", pp. 701 – 706, Proc. International Symposium on Microelectronics, IMAPS, San Diego, CA, Nov. 1 – 4, 1998

[7] Lasky, R. and Morvan, Y., "What is Needed to Establish Flip Chip as a Standard SMT Process", pp. 1517 – 1525, Proc. Of Pacific Rim/ASME; InterPACK 99, June 13 – 19, 1999.