

## The Final Revolution?

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Electronic packaging began over 100 years ago as the glass hermetic enclosure for vacuum tubes and optoelectronic products like the CRT. The glass package was an integral part of the system and the device could not function without this enclosure since a vacuum was required for operation. Later, sealed hermetic metal and ceramic packages were introduced as solid-state devices evolved and electronics proliferated. Modern component packages are the bridge between the semiconductor world and the printed circuit industry that must provide compatibility and protection. The 1960's enjoyed considerable innovation as we began the first Packaging Revolution that sought to reduce cost and size while increasing performance. This revolution adopted plastics that made it possible to automate the packaging process and thus began the long march toward "smaller, faster, cheaper".

During the 1960's, modern packaging concepts evolved as technologists experimented with TAB (Tape Automated Bonding), BGAs (Ball Grid Array), and CSPs (Chip Scale Package). All of these "advanced" concepts were developed early, but were too specialized at this juncture to achieve mainstream status. But the plastic package was also introduced and it had major ramifications. Plastic molded transistor packages, from the late 1950's, evolved into flat packs a few years later to handle ICs. But the flat packs had to be hand-assembled because they were surface mounted packages that couldn't be wave soldered. The surface mount problem was solved by bending flat pack leads at right angles to create a feed-through package that became the popular Dual In-Line Package (DIP). The plastic DIP (P-DIP) was the crucial building block in our first revolution that replaced the costly hermetic packages with non-hermetic plastic. This package also enabled an assembly revolution because boards could now be "stuffed" with DIPs and discrete through-hole packages to be automatically wave soldered.

In the early 1980's, we experienced the next Packaging Revolution, Surface Mount Technology (SMT). Ironically, the 1980's saw the return to surface mount that had not taken firm hold when flat packs and flip chips were introduced two-decades earlier. SMT facilitated major advancements in assembly automation with the added benefits of smaller and more efficient packages. Although the 1980's was the decade of SMT, IBM, followed by General Motors (Delco), used surface mounted flip chips in high volume, starting in the 1960's. Today, SMT is the logical format that brings so many benefits that we can consider it to be a *de facto* standard for the foreseeable future.

The introduction of the Plastic Ball Grid Array (PBGA) brought us into the Area Array Revolution of the 1990's. Yes, we had, and still use, the Pin Grid array (PGA), but a lower cost, solderable area array package made the difference – and launched our 3rd revolution. This format enables high volume manufacturing and considerable design latitude because of the compact footprint. Area array let us shrink down to chip scale size to launch the Chip Scale Package (CSP) that continues to gather momentum and support from all sectors. We now have both flip chips and CSPs that seem to be the ultimate in miniaturization – the end game. But is chip scale area array really the Final Revolution? After all, the package cannot be made any smaller, so where else can we go?

We are not yet done. Borrowing from building architecture and applying common sense, the final package must "rise" to the occasion. We must vertically cluster chips just as builders stack floors to achieve the ultimate density. We've done this quite successfully with dwellings for thousands of years. And we've also been stacking an increasing number of layers inside the IC. The brain, of course, has a 3D architecture housed in a single package.

Today, the stacked chip concept continues to gain popularity as more 3-D designs are announced. The two main strategies are chip-in-package and stacked package constructions as well as combinations. Rigid, flex, ceramic, and all-semiconductor designs are being used. Tessera introduced folded flex CSPs and more designs keep coming. The major packaging foundries offer dozens of stack-ups that use wire bond, flip chip and, combinations. The record stack is now at 10 die and probably climbing. So are we in the Final Revolution? Perhaps! The density dilemma appears to be solved although the work is far from complete. Stacked designs are being applied to chips with lower I/O and modest power but maybe this can be extended. So just how new is the MultiChip Package (MCP)? Well, the MultiChip Module (MCM) has been used since the 1980's, and was described in the 1960's, but designs have been single-plane, not stacked. But 3D package stacking has definitely been around for quite awhile. Early computer buffs may recall *do-it-yourself* package stacking. We doubled memory in the Radio Shack Color Computer (CoCo), and probably other early machines, by piggybacking the DIPs and soldering the leads to the original on-board memory DIPs.

Does anyone see another packaging revolution in the future? We'd like to hear your thoughts.