

## **“No Place to Go but Up”**

Ken Gilleo (with Vern Solberg) EP&P 2002?

We could be talking about the economy or the deflated tech stocks. Actually, the topic is advanced packaging. How can we continue to achieve smaller and denser packaging once the footprint is chip size and silicon utilization is 100%? Can any package be smaller than chip-size? Well, maybe not in the two-dimensional world of area, but the issue is really about density. Architects solved the *dwelling density dilemma* ages ago by stacking floor upon floor culminating in the modern skyscraper. The same stacking principle is an obvious fit for electronics. Today, we are moving toward the “skyscraper era” in high-density packaging, especially for memory. But we’ve been stacking electronics for a long time as subsystems, so let’s briefly tour 3D electronics.

A long time ago (before 1981), there was no IBM PC, but there were some delightful early machines like those in the Radio Shack product line. The pioneering computer user often became a good technician like the early automobile owner who became a pretty good mechanic. Insufficient memory was a big problem with the few-KB chips of that era. One home-brew solution was to piggyback, or stack, additional memory packages on top of the original DIPs (Dual In-Line Package) that came soldered to the motherboard. The DIP was a standard IC package before the SMT revolution. The leads of the top package were hand-soldered to those of the lower DIP. This was a simple way to double the RAM and take your almost-enough 16 KBs to an awesome 32 KB (that’s K for kilo). Today, a quarter-century later, the stacking principle is being applied to bare die.

One of the simplest techniques is to bond a smaller die on top of a larger one leaving enough clearance for wire bonding. This is a nice fit with existing equipment that stays inside of the infrastructure. According to 3D expert Lee Smith, Amkor has over a dozen stacked die packages. Some use a “wedding cake” wire bonded stack as shown in Figure 1. But the stacked die can all be the same size, according to Bob Marrs of K&S. The first die is wire bonded and then the next die is attached on top of the first followed by wire bonding. The process is repeated until the desired stack is obtained. Many other designs are available and some (Cubic) route conductors down the sides of the chip stack.

Flex circuitry can also be used to connect multiple levels. Flex is a great choice since it’s the original 3D circuit where designers think “volume” not just “area”. A good example is the Ford Radio circuit manufactured over 20 years ago. The product used rigidized flex (not the same as rigid-flex) made by bonding non-conductive stiffeners to the component assembly zones of the flex. The circuit was first populated by inserting the feed through packages into openings in the stiffener and wave soldering the flex. The finished circuit was singulated by snapping the circuits out of the frame and folding into a 4-layer stack. The result was a compact module that plugged into a back plane. Field repair was simple; unplug the module, unfold the circuit and work on the components (in a time when there was repair). OK, it’s a nice 3D assembly, but not really a package.

In the late 1980’s, Sheldahl introduced a new multilayer flex process, called Z-Link where double-sided flex circuit pairs were stacked and laminated using Z-axis adhesive to provide vertical connections. During the development stage, ideas emerged that moved closer to packaging concepts. One plan was to add flip chips (flip-on-flex) to layer pairs before lamination. We believed that the conformal nature of flex would permit the stack to be laminated without damage to the chips. The “Flip Chip In Flex” concept was never implemented but may still be a neat idea. Today, one could add solder spheres to make a Z-BGA.

Here’s one final “never implemented” Sheldahl 3D idea called the *4<sup>th</sup> dimension*. A single piece of flex is laminated into a serpentine 3D stack using Z-axis adhesive. The conductive adhesive creates vertical connections, but the “flying tails” also connect layers - this is the 4<sup>th</sup> dimension. Now let’s look at commercialized 3D flex.

Tessera's folded-flex stacked die  $\mu$ BGA<sup>®</sup> package furnishes the lowest profile and outline possible. The folded-flex stacked die package recently announced by Intel includes two distinctive die shapes, a pair of Flash memory die and a single SRAM as shown in Figure 2. The folded-flex uses the same Tessera principles as the  $\mu$ BGA<sup>®</sup> package. This technology relieves mechanical stress, enabling a highly reliable package almost as small as the chip itself. The illustrated cross-section shown in figure 2a details the three-die folded-flex stacked  $\mu$ BGA package with bumped solder contacts. Figure 2b shows an Amkor implementation.

The flexible substrate is folded so as to stack at least some of the microelectronic elements in substantially vertical alignment with one another to provide a stacked assembly with the conductive terminals (solder balls or lands) exposed at the bottom end of the stack. The multiple die folded-flex package (typical of the single die package) is processed as a uniform array in a row and column format. But, instead of singulating only one die unit from the array, the folded flex substrate will retain two, three or more die on a single section of the substrate.

What about the future high-density package? Will we keep stacking higher and higher like the skyscrapers? What kind of vertical connections will evolve? Must we stay with electronic signal paths? Today, we link more and more systems together with "light"; the Internet, offices, aircraft avionics, ship systems and vehicles sensors. So why not use photonics at chip level? An optical channel could handle 1 million times more data than a thousand copper paths! Better yet, silicon is transparent to infrared. Will "light" paths connect stacked die in the future? What do you think?

[Ken Gilleo was R&D director at both Sheldahl and Tessera]

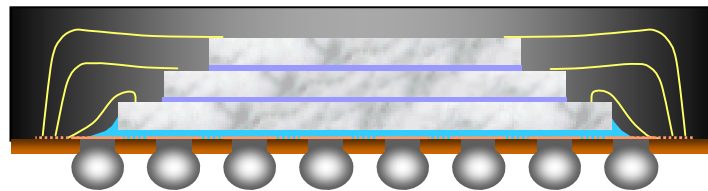


Figure 1 – Amkor's **3S-CSP** Stacked Package (Courtesy of Amkor)

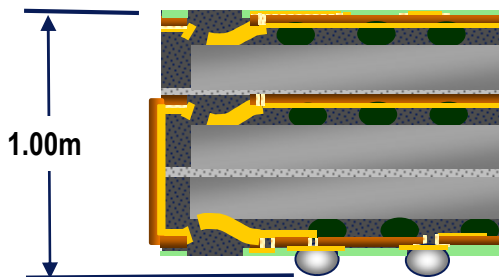


Fig. 2a. - Connections (Tessera)

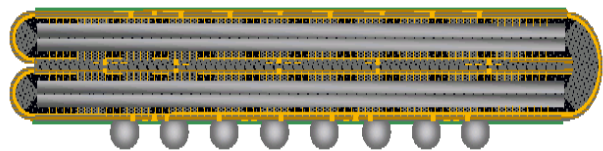


Fig. 2b. - 4 fuBGA (AMKOR)

Figure 2 - 3D Flex Based Packages