Interposer Multilayer Circuitry

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Introduction

Since the first circuit patent filed in 1903, interconnect developers recognized that more than one conductor layer was required. Although circuit technologists agree that multilayers are needed, they have different ideas on how to accomplish the task. Over the years, many clever vertical connection strategies have been proposed and many have been tested. The most common connection method for organic constructions is the through-hole process. Circuits are manufactured and bonded together with adhesive. The stack is drilled and the "through-the-stack" holes are plated to create vertical conduits. Other popular methods include build-up and co-fire processes developed by the hybrid industry. But there have been many others.

Random Interposers

Interposer connections are one logical idea that has not quite caught on. We can define a circuit interposer as a connection material or construction that will electrically and mechanically connect circuit pair layers in the vertical direction without interfering with X-Y plane conductor paths. Perhaps the simplest interposer is Z-axis, or anisotropic conductive adhesives (ACA). In the 1980's, Sheldahl, then the technical leader in flexible circuitry, developed Z-Link®. This was a flex-based multilayer circuit process that used Z-axis adhesive made with solder powder in a B-staged epoxy film. The idea was to mate pairs of double-sided circuits using this film that can be thought of as a special bond-ply adhesive. The circuit stack consisted of circuit pairs with the interposer film placed between layers. The stack was put in a laminating press where heat cured the adhesive and caused the solder powder to permanently connect the opposing bare, OSP-treated copper pads shown in Figure 1. Once bonded, the solder junctions were quite robust and didn't open again, even during reflow. The solder particles formed micro-connections that only got better if the solder was re-melted. Attempts to thermally damage the circuit was akin to trying to open up a solder bridge in a 2-mil gap and it does not happen easily.

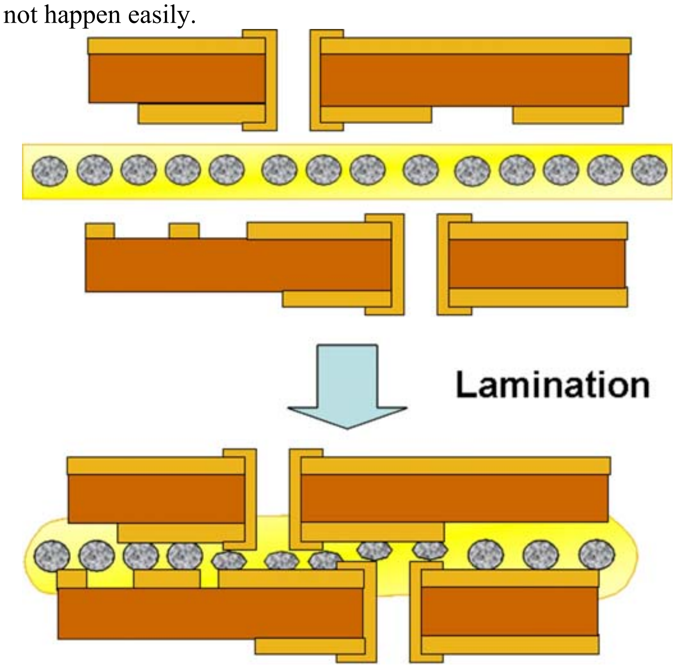

Figure 1 – Z-Link (Sheldahl)

The Z-Link product was good for a starter. You could easily make blind and buried vias by just designing the layer pairs. And it was possible to combine all kinds of different circuit materials. One popular version was constructed by mating small Kapton layers to larger polyester circuits. The idea was to use very low cost, but low-melting Mylar® (polyester), as the main circuit without components. The higher-priced but high-temperature Kapton (Polyimide; PI), could be used as the platform for components since it's easily soldered. The PI assembly, complete with components, could then be bonded to the polyester circuit using the Z-Link adhesive film. The localized heating didn't cause problems for the temperature-limited polyester that can only be soldered with great difficult and special processes. A soft rubber bonder pad prevented component damage, but the bond area was typically along the perimeter away from devices. Sheldahl called it the "Density Patch" and Figure 2 shows a product.

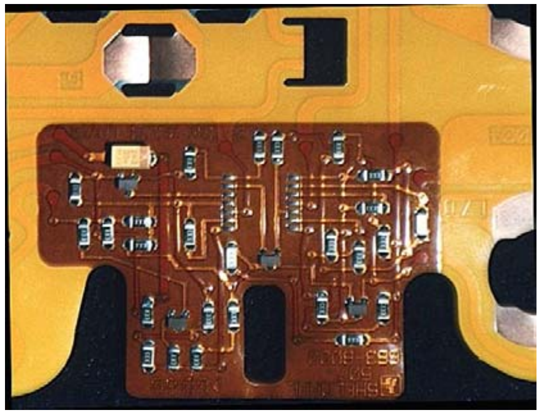

Figure 2 – Density Patch (Sheldahl)

Patterned Interposers

One increasingly critical limitation of Z-Link was the inability to make really dense circuits. The random Z-axis adhesive worked well for low to modest density only. What was needed was a patterned anisotropic conductive adhesive (PACA). A consortium was formed under US government funding and work progressed as Sheldahl, CTS, Delco, and other companies developed and tested new kinds of interposers. The work appeared to be reasonably successful and the published reliability data looked good. CTS Corporation called the process "co-lamination" to link it with the "co-fire" process from hybrids. But funding ended and no commercial products were launched.

In the early 1990's Tessera worked on Interposer type multilayer modules. Tessera initially wanted to be a Multi-Chip Module (MCM) company, but was not able to continue funding both module and chip carrier development and thus opted for CSPs. The Tessera idea also focused on flex because of its thinness, compliancy and proven high-density ability. Tessera used a conductive adhesive to create vertical connection columns. Microvias were lased through flex bond-ply (polyimide with dry film adhesive on both sides). The silver-filled adhesive was applied into the vias and B-staged or cured, in the case of elastomers. Double-sided circuit pairs could be bonded with the interposer films to make high-density modules. The work was shelved to focus on the µBGA that was starting to attract attention, so the invention never got a fair test.

Interposers Today

So is interposer multilayer a good idea today? Perhaps. As density goes up, better vertical connection methods are needed. So why not use some form of PACA? Perhaps it could be some combination of the Sheldahl and Tessera concepts along with others. It seems likely that the random interconnect isn't dense enough and Z-Link really did get a fair chance (received R&D 100 Award). So could we make a high-density patterned interposer that would enable economical circuits and modules? And what would it look like? The idea of a metallurgical connection made with solder has more appeal than adhesives. The Tessera laser via fill idea also has merit. Maybe the product could have vias filled with a solder-based or solder-like material. So is anyone working on such a passed over idea?

Sumitomo Bakelite recently announced a product called SIZUC for Simultaneous Interconnect Z-Axis Technology for Uniform Conduction. OK, maybe the name needs a little work, but what is the product? The dielectric is a solder connection resin with fluxing capability. The conductor is lead-free solder. We'll have to wait for more information, but the interposer idea is still a good one and needs another chance.

Does this product sound like the original Z-Link? Perhaps it should since SB was Sheldahl's partner during Z-Link development in the mid-1980's.

Buried Via and Chips?

Before ending, let's look at some of the ideas "buried" within the Z-Link idea. As they say, "Inside every idea is a better idea trying to get out", or in this case, "in". Sheldahl had plans for Z-Link beyond just a replacement for drill & plate multilayer. One idea was to populate circuit layers with small chips and then laminate them into the stack. Flip chips on flex were being tested at the time, so why not put active devices inside the layers. Certainly, it would make sense to also add passives, either as a layer material or as discretes. No work appears to have been published on embedded ML, but it was widely discussed at conferences. Maybe this is the right time to turn things inside out or visa versa.

And now, the 4th Dimension

But there was at least one more cute idea and it answers the question posed by Dominique Numakura a few months ago in this magazine, "Can we have 4-dimensional circuits?" Sure we can! OK, how? The answer is buried within Z-Link and flexible circuitry. Just use one continuous double-sided flex circuit for the stack. Don't cut it, just serpentine as shown in Figure 3. The external loops between layers are the 4th dimension and that's what Sheldahl called it back in 1985. OK, the loop is really X and Y bent into the Y plane, but it provided another means of moving from layer to layer. In fact, one design looped the top layer to the bottom so that these two were connected without passing through the middle. Now what if we add those embedded chips to the serpentine circuit? You get bare die and a folded flex chip carrier. Does this old idea remind anyone of the new Tessera 3D carrier shown in Figure 4? So let's keeping thinking, turning problems inside out, and stay *flexible*!

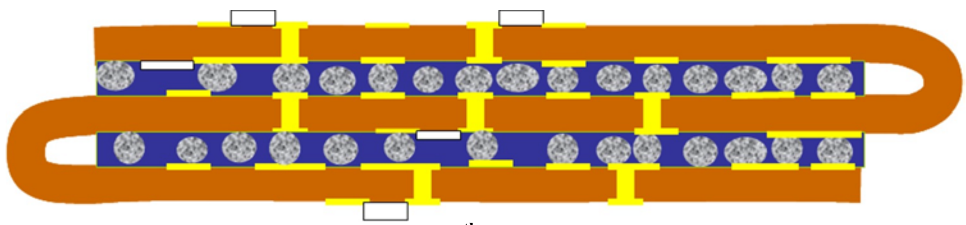

Figure 3 – The 4th Dimension Circuit

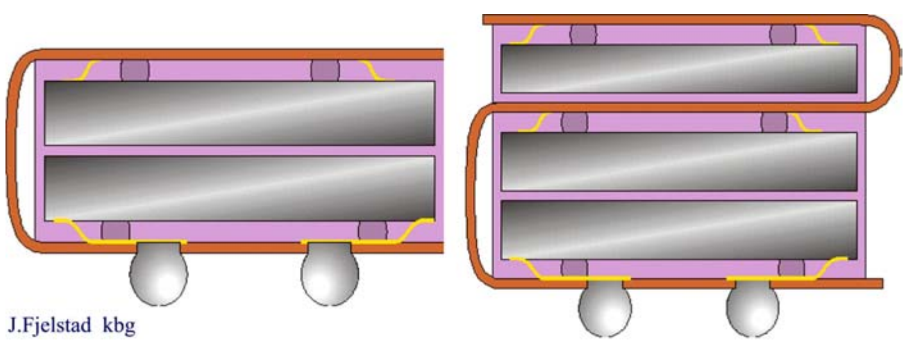

Figure 4 – New 3D Flex CSP (Tessera)

Note: the author worked on interposers at both Sheldahl and Tessera